AN10962

Dimmable CFL using the UBA2026X family

Rev. 1 — 4 April 2012 Application note

Document information

Info	Content
Keywords	CFL, step dimmable, UBA2026X
Abstract	This application note describes the design of a dimmable Compact Fluorescent Lamp (CFL) with low dimming level using the UBA2026X.

Revision history

Rev	Date	Description
v.1	20120404	first issue

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1. Introduction

This application note describes the design of a step dimmable Compact Fluorescent Lamp (CFL) with low dimming level using the UBA20260 or UBA20261/2. A 20 W application where the UBA20260 is used with external MOSFETs. For power levels up to 18 W, the UBA20261/2 with integrated MOSFETs can be used. The UBA2026 controller can be used with both the 120 V (AC) and 230 V (AC) mains voltage applications. Optimal performance is obtained when the UBA20261 is selected for use with 120 V (AC) mains applications. The UBA20262 provide optimal performance with 230 V (AC) mains applications.

Remark: Unless otherwise stated all voltages are AC.

A Voltage Source Charge Pump (VSCP) is added to the circuit to ensure that the applications power factor is greater than 0.6 at all dimming levels. A no-lamp detection/protection circuit has been added externally to the main board for evaluation in a laboratory set-up with different burners. However, when the lamp ballast plus burner are enclosed in the CFL housing, the no-lamp circuit is not necessary.

2. Scope

This application note is organized as follows:

- Section 3 describes the basic operation of step dimming
- Section 4 describes application design
- Section 5 Appendix 1: power calculation equations
- Section 6 Appendix 2: MOSFET current calculations

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3. Step dimming block diagram

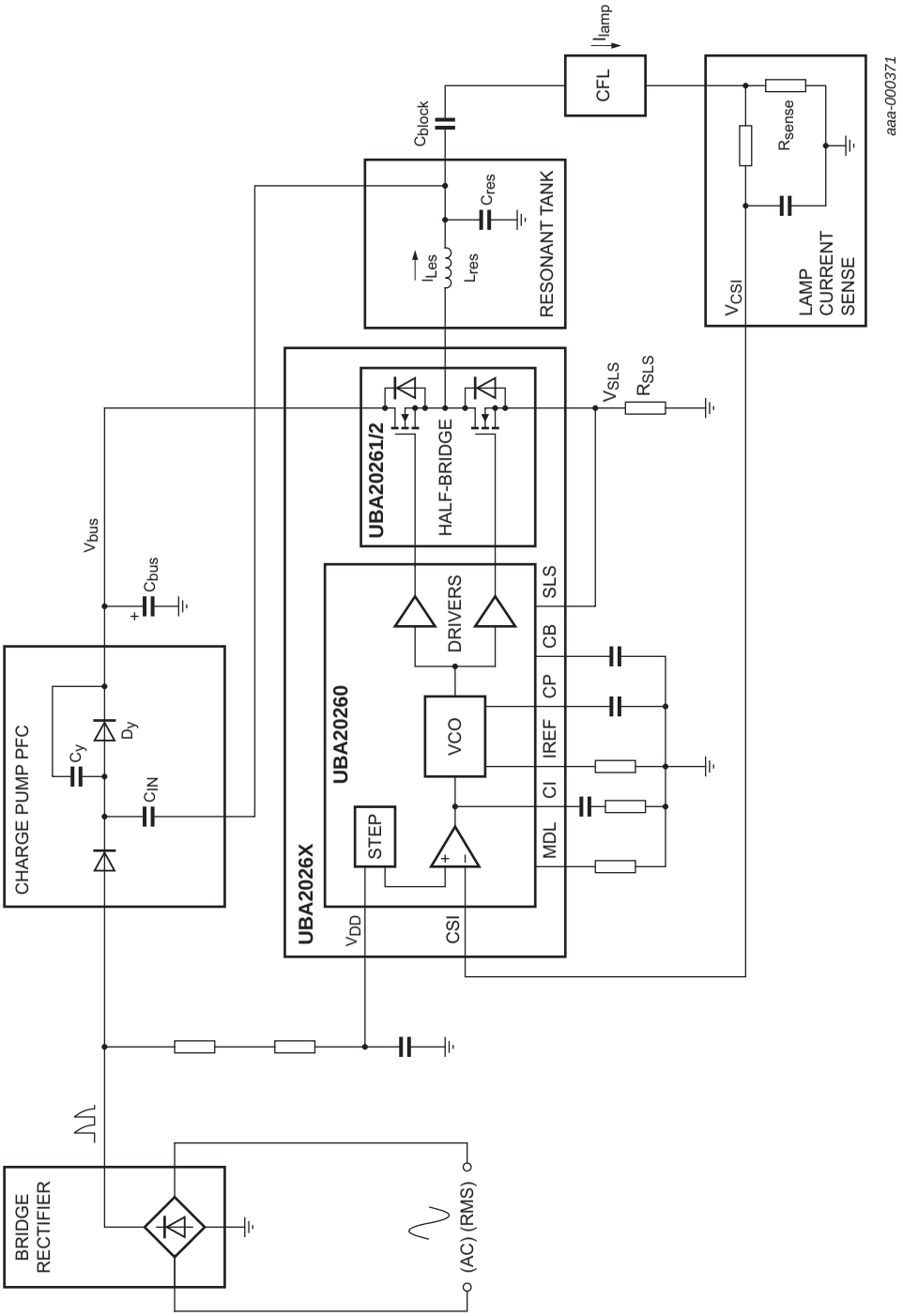

Fig 1. Block diagram of a high PF dimming CFL and UBA20261/2 controller

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4. Application design

4.1 Simplified circuit diagram

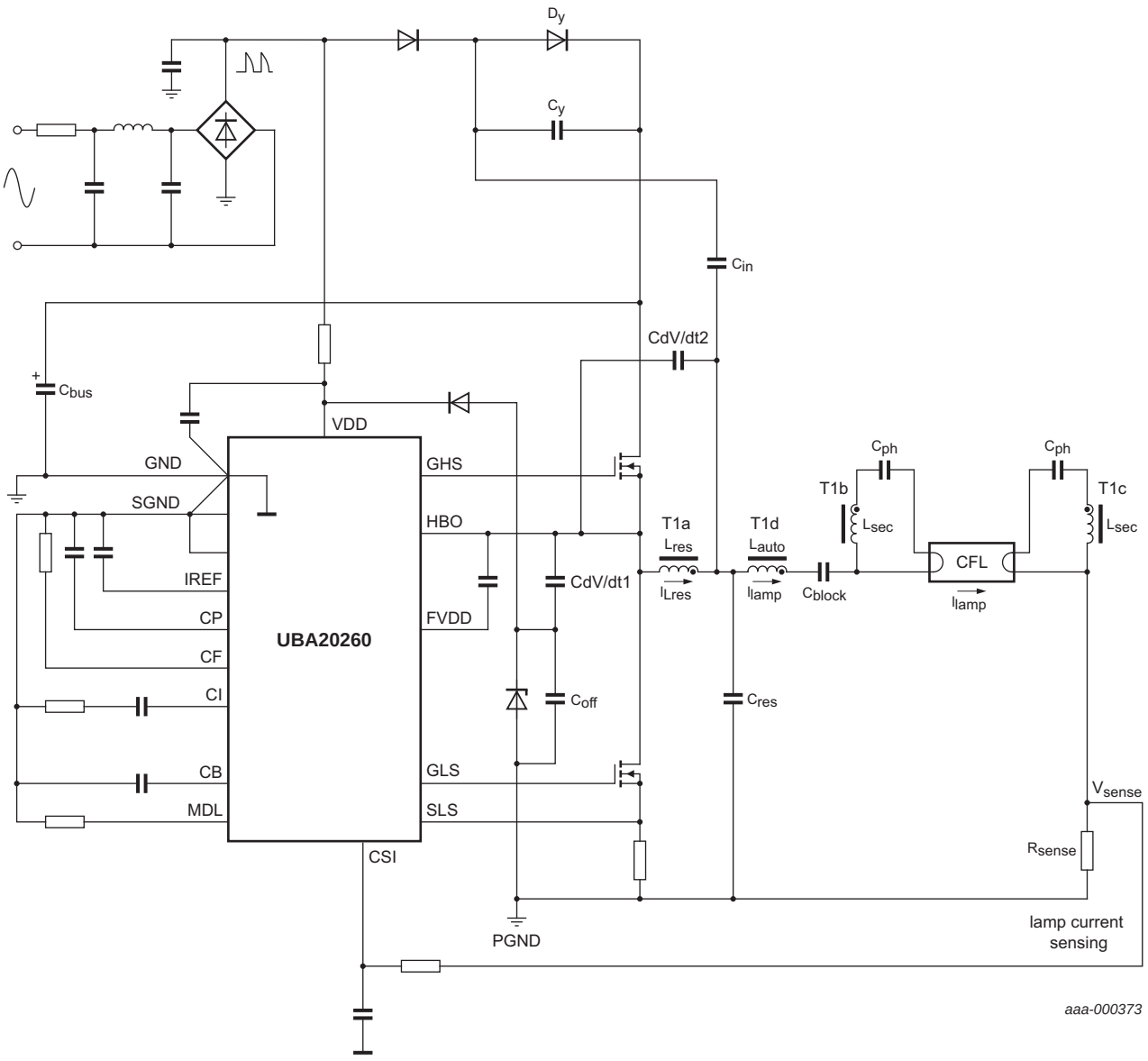

Fig 2. Block diagram of a high PF dimming CFL and UBA20261/2 controller

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4.2 Resonant tank parameters

The resonant inductor (L_{res}) is the dominating component for the power delivered to the lamp (P_{lamp}), however, the resonant capacitor (C_{res}) also has influence. Calculate the L_{res} value to deliver the required lamp current during the boost period. The lamp current during boost is 1.5 times the nominal lamp current. C_{res} is calculated to ensure that the operating frequency is above 40 kHz in the boost state and the minimum mains voltage is V_{mains} −10 %.

The current in the MOSFETs increases for larger a C_{res}. At a smaller C_{res}, the possibility of hard switching increases because the resonant tank is no longer inductive.

An important parameter is the parasitic capacitance inside the transformer L_{res} and its secondary windings. Parasitic capacitance is especially important for the filament winding connected to the lamp current sense resistor R_{CSI}. Due to parasitic capacitance, current is directly injected from the resonant tank into R_{CSI}, bypassing the lamp discharge current.

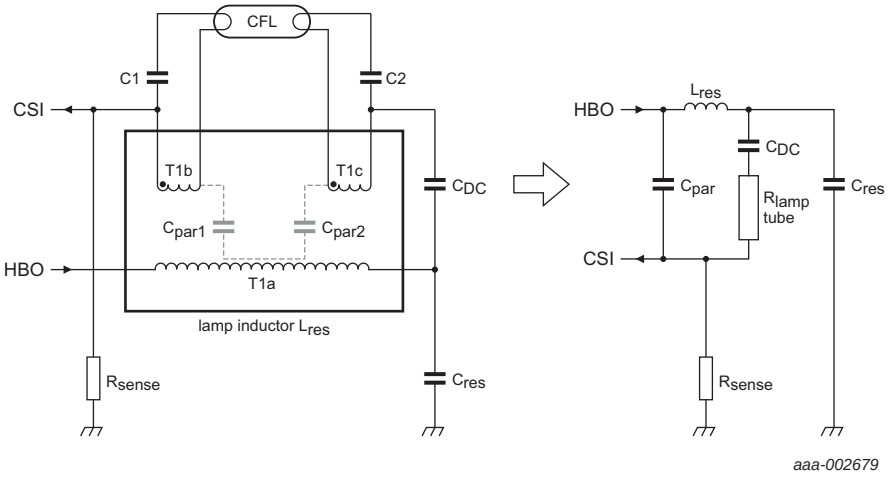

Fig 3. Transformer model L_{res} with parasitic capacitors C_{par}

This current degrades deep dimming performance because the lamp discharge current is no longer regulated. To ensure good deep dimming performance, the parasitic capacitance must be less than 25 pF.

When the autotransformer winding is used in series with R_{CSI}, the capacitance between L_{res} and winding T1d must be less than 25 pF. See Section 4.3 for more information.

Table 1 and Table 2 list the resonant tank parameter starting values for 230 V and 120 V mains.

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Table 1. Resonant tank values 230 V mains

Applicable to all values: C_{res} = 2.2 nF, C_{block} = 47 nF and C_{IN} = 2.2 nF.

P_{IN} (W)	P_{lamp} (W)	V_{lamp} (V)	I_{lamp} (mA)	L_{res} with boost (mH)	L_{res} without boost (mH)
15	13	105	120	2.5	2.7
18	16	100	160	2	2.5
20	18	110	160	2	2
23	21	110	190	2	2

Table 2. Resonant tank values 120 V mains

Applicable to all values: C_{block} = 22 nF and C_{IN} = 3.3 nF.

P_{IN} (W)	P_{lamp} (W)	V_{lamp} (V)	I_{lamp} (mA)	L_{res} with boost (mH)	L_{res} without boost (mH)
13	11	100	110	1.2[1]	1.2
15	13	105	120	-	1.2[1]
15	13	105	120	1	-[2]
20	18	110	160	-	1[2][3]

[1] C_{res} = 3.3 nF.

[2] C_{res} = 4.7 nF.

[3] Not recommended for resonant topology. Use voltage doubler topology instead.

4.3 Autotransformer

The autotransformer concept lowers the MOSFET current by reducing the voltage on C_{res} while maintaining the nominal lamp voltage. An autotransformer is a transformer that is tapped somewhere on the primary winding to generate a lower secondary voltage. Since a transformer works both ways using the center tap as primary, you can also raise the voltage. The disadvantage of the autotransformer is that the primary and secondary are non-isolated. However, when use in a CFL application, this fact is not a problem.

The autotransformer concept is shown in Figure 2, where T1a and T1d are the autotransformer primary and secondary windings.

The auto-transformer concept is mainly for the 120 V resonant topology. The concept reduces the reactive half-bridge loading by lowering the voltage on the resonant capacitor. In doing so, overall efficiency improves by 30 %.

When a burner with a low lamp voltage (< 95 V) is fitted, the same topology can increase the lamp voltage on the resonant capacitor. The topology ensures that the voltage source charge pump can generate the required hold current.

In all applications, the output voltage of the secondary winding of the autotransformer is set at 20 V (RMS). The nominal lamp voltage increases/reduces, depending on how the primary and secondary winding are added in series.

Remark: If the voltage is increased/reduced, note the dots in the transformer windings because they determine how the windings are used in the schematics: Figure 12 and Figure 13.

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Use the autotransformer for 120 V mains in two cases and when the nominal lamp voltage is:

- > 110 V: to lower the voltage on the resonant tank
- < 95 V: to increase the voltage on the resonant tank

Table 3. Transformer ratios for 230 V and 120 V mains

L_{res} with boost (mH)	T1d ratio (L_{res} : T1d)	L_{res} without boost (mH)	T1d ratio (L_{res} : T1d)
Transformer ratio 230 V			
2	9.74 : 1	2.5	9.44 : 1
2.5	9.44 : 1	2.7	10.27 : 1
Transformer ratio 120 V			
1	7.26 : 1	1.2	6.84 : 1

4.4 Inductive mode preheating and SoS

Correctly preheating the filament is necessary to ensure long lamp operating life and provides the advantage a lower ignition voltage.

The preheat time is applied to the filaments during the preheat period and is set using Equation 1:

$$t_{ph} = \frac{C_{CP}}{I_{o(CP)}} \times \left(\frac{16 \times V_{hys(CP)}}{5 - V_{th(CP)max}}\right) \quad (1)$$

Where: C_{CP} = 330 nF, $I_{o(CP)}$ = 5.9 µA, $V_{hys(CP)}$ = 0.7 V, and $V_{th(CP)max}$ = 4.5 V. The preheat time is 0.67 s.

The preheat frequency can be set by measuring the voltage across the SLS resistor between the source and ground of the lower MOSFET. See Figure 1. The half-bridge frequency starts at $f_{VCO(max)}$ and sweeps down until the voltage on the SLS pin reaches the V_{ph} level that is defined in the specification. The sweep then stops for the duration of the preheat time t_{ph}.

During the preheat time, the frequency is controlled so that the voltage on the SLS pin stays constant, implying that the half-bridge current is kept constant. The half-bridge current level can be adapted by changing the value of the SLS resistor. However, the value selected must not cause the lamp to ignite during the preheat time. Also the saturation protection and overcurrent protection use the same resistor. Both of which can be triggered too soon. Therefore, practical values for R_{SLS} for 120 V mains are between 0.9 Ω and 1.5 Ω. Values for 230 V mains are between 1.5 Ω and 2.2 Ω. Too low a value and during low mains, the open lamp voltage is too high. Too high a value and saturation protection is triggered.

If the preheat energy or SOS are not within limits, adjust the secondary turns or the secondary capacitors.

The frequency versus time is shown in Figure 4.

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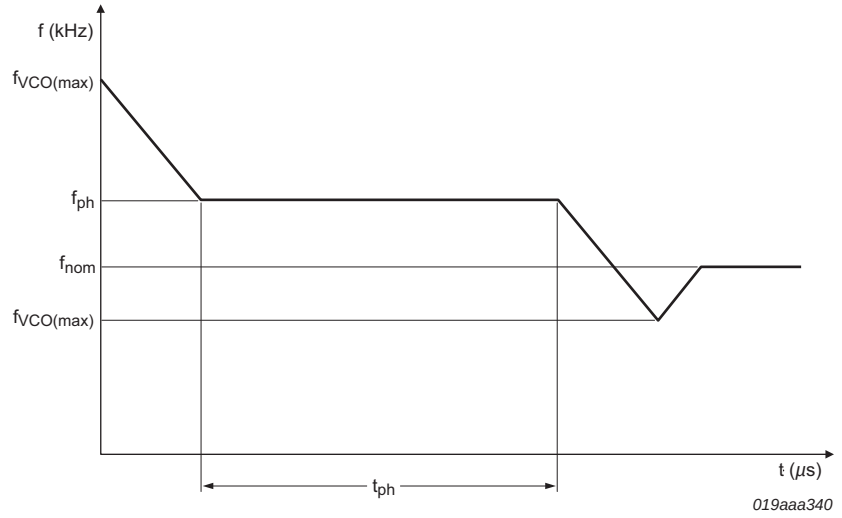

Fig 4. Frequency versus time during start-up

For inductive mode heating, the relationship for the preheat (filament) current is calculated in Section 6.

For example, when the half-bridge frequency is 71 kHz, non-overlap time is 1.5 μs and the RMS filament current is 0.25 A. Then the filament power dissipated is approximately 1.6 W when the hot filament resistance R_{filter} = 25 Ω. The power supplied to the filament during preheat is $f_s CV^2_{sec}$ and for a capacitance of 47 nF:

$$V_{sec} = \frac{V_{pri}}{n} \tag{2}$$

where V_{pri} = 350 V and:

$$n = \sqrt{\frac{L_{res}}{L_{sec}}} = 16 \tag{3}$$

Then power supplied to filament is approximately 1.6 W.

To guarantee sufficient filament current is provided at the end of the preheat period, the hot to cold ratio of filament resistance must be preferably 4.75 : 1. If however, this conflicts with the SOS at deep dimming, choose a lower value of 4 : 1. A higher value can overload the filament and reduce the operating life time. After the preheat period, the frequency falls and the lamp ignites when the ignition frequency f_{ign} is reached. The lamp can be modeled now as a (negative) resistance where:

$$R_{lamp} = \frac{V_{lamp}^{\ 2}}{P_{lamp}} \tag{4}$$

Before ignition, the lamp has a much higher impedance as no lamp current is flowing. Both characteristics are shown in Figure 5.

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Capacitor C_{CF}, resistor R_{IREF} and the voltage at the CI pin determine the internal Voltage Controlled Oscillator (VCO) frequency (half-bridge frequency). The minimum and maximum frequencies are as defined in Equation 5:

$$f_{VCO(min)} = 40.5 \times 10^{3} \cdot \left(\frac{100 \times 10^{-12}}{C_{CF}}\right) \cdot \left(\frac{33 \times 10^{3}}{R_{IREF}}\right) and\ f_{VCO(max)} = 2.5 \times f_{VCO(min)} \quad (5)$$

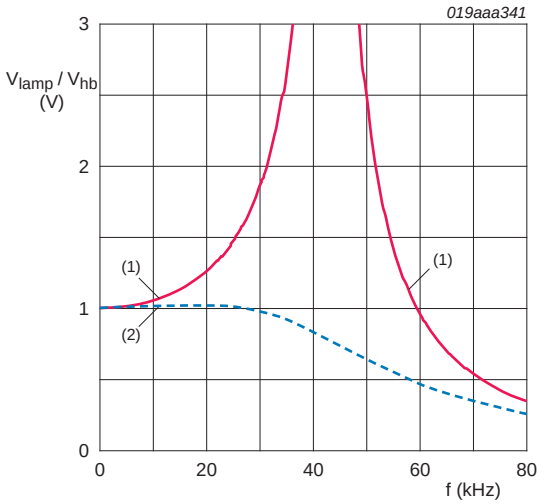
If P_{lamp} = 20 W, V_{lamp} = 110 V; $L_{res} = 2 \cdot 10^{-3}$, $L_{sec} = 10 \cdot 10^{-6}$, $C_{sec} = 33 \cdot 10^{-9}$ and $C_{res} = 4.7 \cdot 10^{-9}$

$$R_{lamp} = \frac{V_{lamp}^{2}}{P_{lamp}} = 605\ \Omega \quad (6)$$

$$C_{p} = 2 \cdot C_{sec} \cdot \frac{L_{sec}}{L_{res}} = 2.4 \times 10^{-10} \quad (7)$$

$C_p = 2.4 \times 10^{-10}$

$\omega(f) = 2 \cdot \pi \cdot f$ and $p(w) = j \cdot w$.



(1) H(2·π·f 2000) lamp not ignited.

(2) H(2·π·f 605).

Fig 5. Transfer of frequency before and after ignition

After lamp ignition, the filaments must have enough supplied power in order to maintain an optimum temperature over the complete dimming range. Too low a temperature and sputtering or local hot spots occur resulting in damage to the filament. Too high a temperature causes evaporation of the filament over a longer period. The Sum of Squares (SoS) is a measure of the expected amount of heat generated in the filaments and is expressed as $SoS = I^2_{LL} + I^2_{LH}$. Figure 6 shows the waveform direction of I_{LL} and I_{LH} against time for period the filaments are inductively preheated.

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SoS must remain between the lamp manufacturer specified minimum and maximum setting. However, a SoS setting close to the target setting is preferred for optimal long life operation of the lamp. Maintain within specification adequate filament preheating and optimum SoS but in practice, they are conflicting requirements. Further information can be found in Ref. 2.

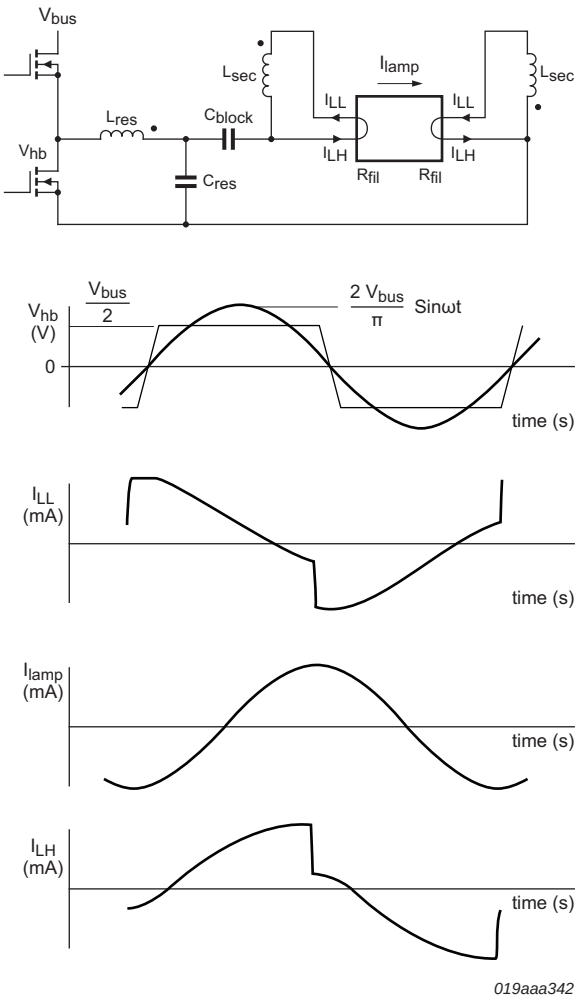

Fig 6. Lamp filament currents for inductive mode heating

4.5 Charge pump and design considerations

To maintain a power factor of PF ≥ 0.6 without using bulky filter components operating at mains frequency, needs a different solution to correct the power factor. The solution is a charge pump.

A charge pump converter is normally use to obtain a power factor of 1, this is also called a unity power factorCharge Pump Power Factor Correction (CPPFC). In this application, trade-offs are made to minimize the extra components in the charge pump circuit and the required application power factor. The extra components are not only more expensive power components but they need more board space which is limited in CFLi applications.

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The most cost-effective and easy solution is a Voltage Source Charge Pump (VSCP) as described in Ref. 1. However, three problems exist in VSCP electronic ballasts:

- high Crest Factor (CF)
- its inability to meet the unity PF condition automatically
- high bus voltage stress in light-load operations such as preheat

To improve the lamp CF, minimize the modulation effect of C_{IN}. To achieve modulation effect reduction, the original capacitor C_{IN} is split into two capacitors C_{in} and C_y. Capacitor C_y is in parallel to D_y, as shown in Figure 1. In the equivalent tank, capacitors C_{IN} and C_y are in series which reduces the equivalent capacitance (see Section 5).

This circuit is called the VS-CPPFC electronic ballast with Improved Crest Factor (ICF). As C_{IN} is divided over capacitors, the high frequency charge pump source voltage is divided as well. Consequently, the V_{lamp} or the voltage across C_{res} is also divided. This leads to much lower voltage stress on V_{bus} than with a basic VSCP.

The voltage stress is important because unlike in triac dimmable lamps, the input voltage is constant over all dim steps. At light loads and when the voltage across C_{res} is high (during the preheat state), excess energy from the charge pump is stored in capacitor C_{bus}. In this situation, the bus voltage can exceed the capacitor voltage.

The design objective is to find the charge capacitor values and the resonant components L_{res} and C_{res}. Take the following factors into account to ensure that the CPPFC electronic ballast design is optimal.

- Limit the maximum DC bus voltage to the 400 V buffer capacitor voltage rating
- meet power factor condition PF $\geq$ 0.6
- Maintain ZVS
- Input and output power balance

The design guideline for the VS-CP electronic ballast with improved crest factor is:

- Set lowest dim setting or monitor the bus voltage during preheat
- Set input voltage to the nominal line voltage +10 %
- Charge pumped bus voltage = $V_{bus} \leq$ 400 V
- At nominal power (no dimming) PF $\geq$ 0.6

See Section 5 for detailed design equations

Typically the power factor of the presented design is:

- PF $\geq$ 0.6 at 100 %
- PF $\geq$ 0.65 at step 1
- PF $\geq$ 0.7 at step 2
- PF $\geq$ 0.7 at MDL

If a higher PF and lower mains harmonic distortion are needed, a VSCP with low frequency second resonance is an option.

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4.6 Step dimming and lamp feedback current

Step dimming of the IC is performed by toggling the voltage on the VDD pin within a set time. The discharge of capacitor CCP connected to the CP pin determines the time slot used to set the next dim step. A value of 330 nF sets the time to 2 s.

Do not connect the start-up resistors R7 and R8 to the normal DC bus voltage to allow good toggling. (See Figure 12 and Figure 13.) Connect the resistors to the rectified mains voltage. The slow discharge of the buffer capacitor does not influence this method of toggling the VDD pin.

When the IC is in the burn state, the internal average current sensor at the CSI pin is compared with one of four internal reference voltages. The CSI pin voltage is derived by sensing the lamp current and converting it to voltage using a sense resistor as shown in Figure 1. This voltage is supplied to the CSI pin as $V_{i(CSI)} = I_{lamp(RMS)} \cdot R_{SENSE}$. The high frequency feed through in the transformer and ignition spike is reduced by adding low pass filter. After R_{SENSE}, the −3 dB point of the filter is set to1.5 MHz.

The maximum voltage on the CSI pin is clamped at 1 V (RMS). The nominal lamp current is calculated using $I_{lamp(RMS)} = 1/R_{SENSE}$.

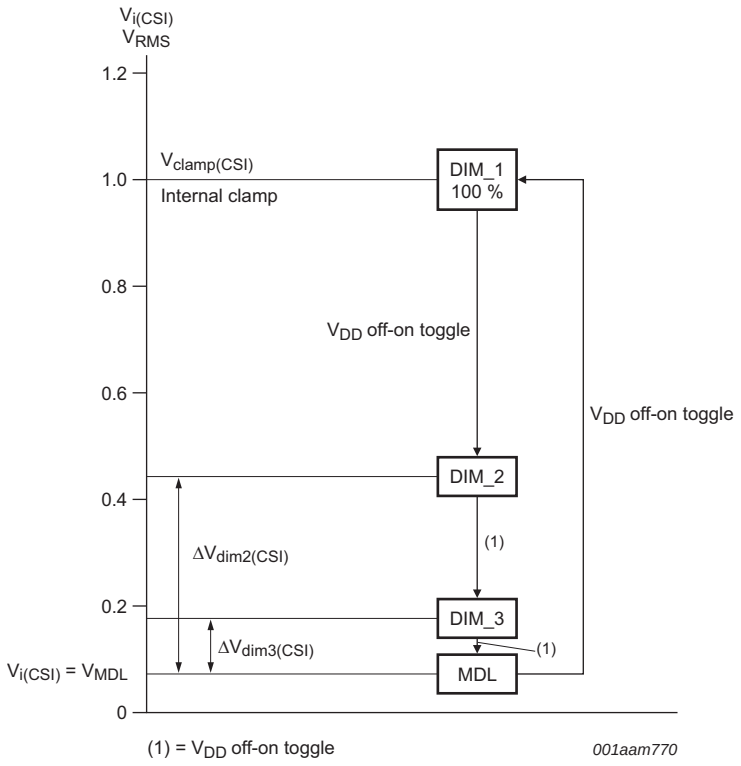

Fig 7. Step dimming levels

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4.7 Setting Minimum Dimming Level (MDL)

The minimum dim level is the dim level of the 4th step in the step dim cycle. It also sets the dim levels of steps 2 and 3 because they are coupled to the MDL level with fixed offsets. Always adjust the MDL to a level high enough to prevent the lamp from switching to the glow phase.

Glow is observed when there is some light coming from the lamp but the CFL tube is not fully lit. This effect also causes flicker when the lamp changes from glow to burn constantly. The MDL voltage is set using R_{MDL} as follows $V_{MDL} = R_{MDL} \times I_{MDL(src)}$ and is lamp-dependent.

Typically, the MDL resistor is set at 1 kΩ which sets the following dim steps:

Table 4. MDL dim level steps

Dim step	Relative lamp current (%)	Relative light output (%)
1	100	100
2	38	60
3	13	22
MDL	3	3

[1] 100 % = nominal lamp current and light output.

4.8 Boosting of the lamp

Amalgam lamps switched on after ≥12 hours have during the first 3 minutes (180 s) a slow run up and less light output. To minimize the problem of slow run up time, the lamp current is increased during the boost time with the fixed 1.5: 1 ratio. The capacitor on the CB pin (C_{CB}) sets the boost time and is calculated using Equation 8.

$$t_{bst} = \frac{C_{CB}}{I_{o(CB)}} \times (126 \times V_{hys(CB)} + V_{th(CB)min} - 0.6) \quad (8)$$

Where: $I_{o(CB)}$ = 1 µA, $V_{hys(CB)}$ = 2.5 V, $V_{th(CB)min}$ = 1.1 V and C_{CB} = 150 nF.

These parameters lead to a boost time of 48 s. Short-circuiting the CB pin to ground turns off the boost circuit.

During boost, the filament current still operates within the SoS limits, to avoid degrading the lamp operating life. If the lamp does not have higher current rated filaments (not intended for boost), then:

- reduce the lamp operating current to 80 % of nominal
- run boost at 1.25 % of nominal

In simple terms, run a 12 W burner at 10 W nominal and 15 W during boost.

Set the power use the full 150 % with higher rated lamps. For example, use an 18 W burner for a 12 W lamp because the filaments automatically have a higher rating.

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4.9 IC supply and ZVS

The IC starts when its supply voltage V_{DD} exceeds $V_{DD(start)}$. Resistor $R_{start-up}$ completes the first charge of the supply decoupling capacitor C_{VDD}. This resistor must be large enough to supply at least 0.32 mA at 12.5 V. The half-bridge begins to switch and the IC is then supplied via capacitor that is connected at the half-bridge as shown in Figure 8. Connect the start-up resistors to the rectified mains, not to V_{bus}. See Section 4.6 for detailed information.

A larger capacitor is required when more current is required in the external MOSFETs and thus in the internal drivers which drive the external MOSFETs. However, if $C_{dV/dt}$ is too large, hard switching or non-zero voltage switching at higher frequencies can occur. The minimum value is calculated using:

$$C_{dV/dt} = \frac{\left(2 \times the\ gate\ charge\ of\ the\ MOSFETs + \frac{I_{DD}}{f_{bridge(min)}}\right)}{V_{bus(min)}} \quad (9)$$

A 470 pF capacitor value is a good compromise between these two situations. A 12 V Zener diode clamps the voltage and supplies V_{DD} via a fast switching diode.

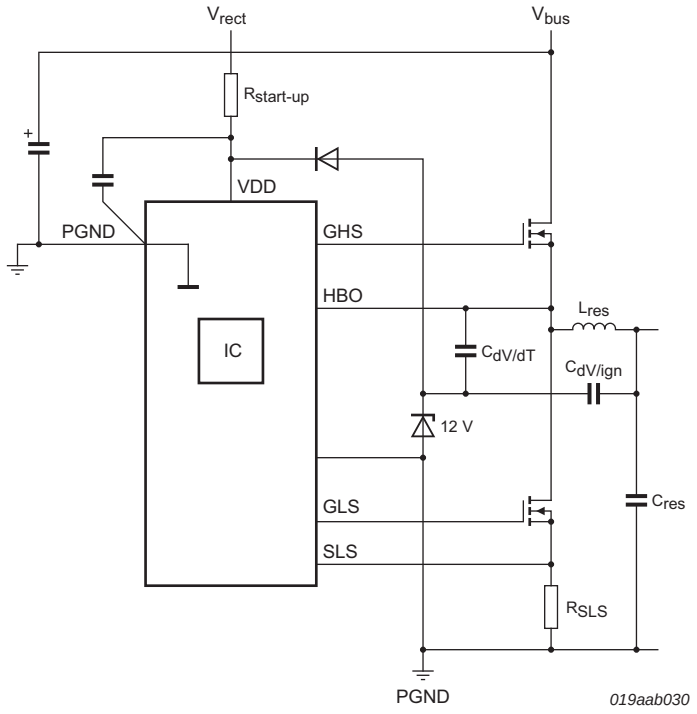

Fig 8. IC supply circuit

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4.9.1 Capacitive Mode Protection (CMP)

The UBA2026X checks capacitive mode operation by measuring the voltage on the SLS pin. Typical waveforms are shown in Figure 10. If the voltage across $R_{SLS} \geq -5$ mV after preheat, the CMD circuit assumes capacitive mode operation when the LS MOSFET is switched on.

To counter this operation, the half-bridge frequency is increased cycle-by-cycle. The frequency increases until capacitive mode is no longer detected. The system can operate safely near the capacitive mode level.

Detailed description of capacitive mode protection mechanism can be found in the *UBA2026x data sheet*.

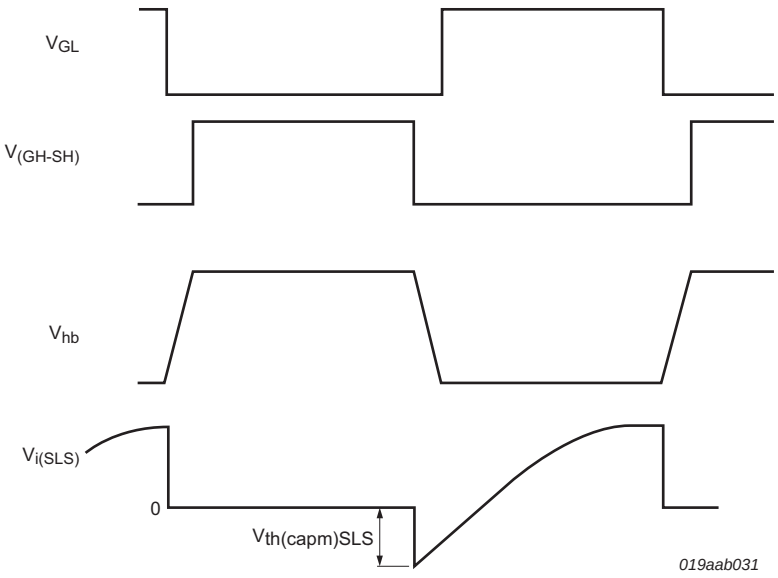

Fig 9. IC supply circuit

4.9.2 Mains input filtering

A Resistance, Inductance, Capacitance (RLC) filter is used to filter the mains. The filter maintains high ElectroMagnetic Interference (EMI) performance at the half-bridge frequency, across the harmonic range. The inductor blocks the HF boost current, while the capacitor provides a low ohmic path for this current. HF current damping can be determined using Equation 20.

$$20\log\frac{1}{(1+\omega^2 LC)^2+(\omega RC)^2} \quad (10)$$

Where: L = 4.7 mH, C = 100 nF and R = 10 Ω.

Then damping at 45 kHz relative to 50 Hz is more than 60 dB as shown in Figure 10 [a]

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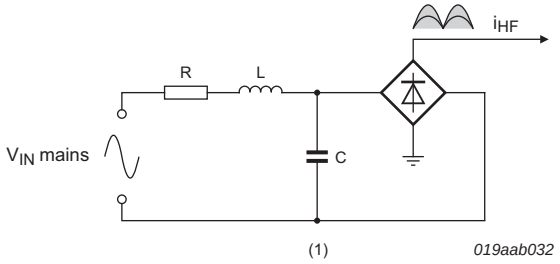
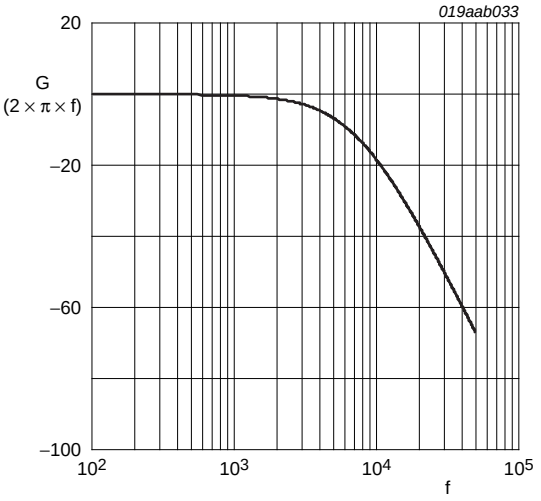


a. Mains filter components.



b. Bode diagram of the filters transfer function.

Fig 10. Mains filter and bode diagram of the filter transfer function

The fused resistor R = 10 Ω is used to limit/dampen the inrush current during start-up. Further information can be found in Ref. 1.

4.9.3 Coil saturation protection and overcurrent protection

The resonant tank inductor is one of the largest components in the application. It is therefore, practical to select the smallest inductor possible. Since the maximum current capability of a coil is only important at power-up, choose a parameter that is sufficient under CFL cold start conditions.

During warm starts coil parameters are different because the core material degrades at higher temperatures. These conditions often lead to coil saturation when the CFL is ignited. This in-turn leads to excessive dissipation of the half-bridge MOSFETs or even the destruction of the MOSFETs.

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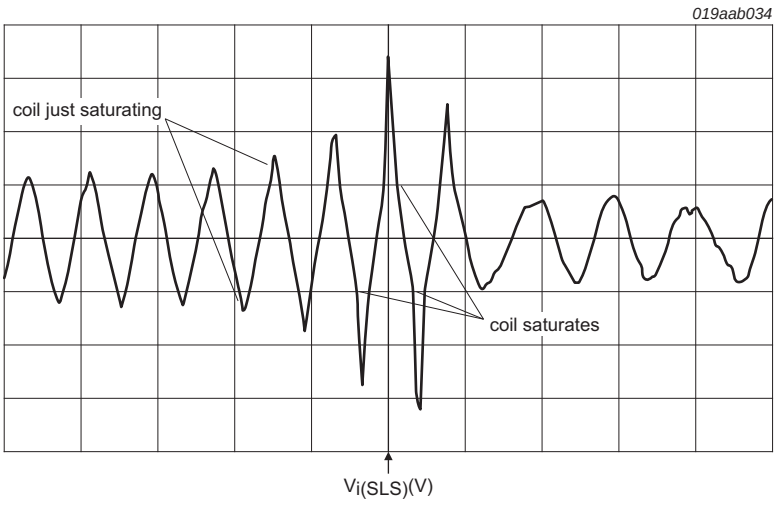

Fig 11. Coil saturation

The UBA20261/2 is equipped with coil saturation protection which enables the use of small inductors in the resonant tank and the inverter without destroying the power MOSFETs.

The circuit monitors the current through the LS MOSFET source. If the current is greater than a factor of 2.5 V of the current during ignition, the IC limits the frequency decrease. Source resistor R17 sets the ignition current (see Figure 12 and Figure 13). If the lamp does not ignite within 25 % of the preheat time, the UBA2026X shuts down.

The coil saturation threshold of the UBA20261/2 is adjustable to allow lower saturation current and overcurrent limits. Typically, the UBA20260 saturation and overcurrent limits are set to the maximum of 2.5 / R_{SLS}. The limits for the UBA20261/2 can be lowered to: (I_{Lsat}*R_{Lsat}) / R_{SLS} where I_{Lsat} = 25 μA. R_{Lsat} cannot be made 0 or grounded. When R_{Lsat} is not used connect a 1 nF capacitor between ground and this pin.

4.9.4 OverPower Protection (OPP)

Since the measured lamp current is clamped at 1 V (RMS), the lamp current remains nominal during mains voltage fluctuations. During over voltage conditions, the half-bridge frequency increases to maintain lamp current constant. Maintain a 10 % higher voltage level on the DCI pin than the required maximum of 1.34 V. This action solves AC line voltage changes in under power situations.

4.10 20 W step dimmable CFL schematic with UBA20260

The full schematic of the application with a 20 W step dimmable CFL is shown in Figure 12.

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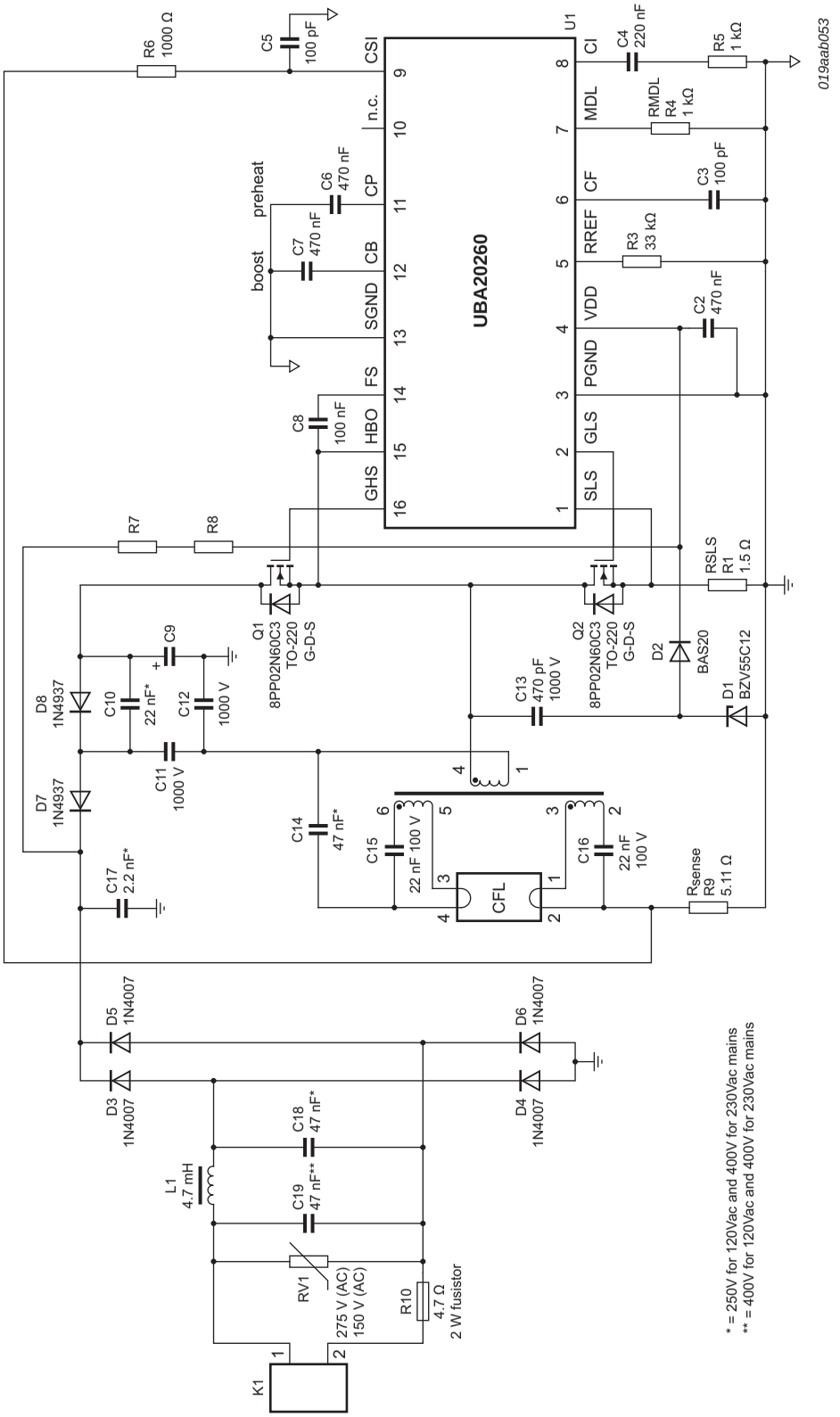

Fig 12. 20 W step dimmable CFL schematic with UBA2026X

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Table 5. Component values

230 VAC mains		120 VAC mains	
Component	**Value**	**Component**	**Value**
R2	not used	R2	not used
C9	6.8 μF; 400 V	C9	22 μF; 250 V
C10	10 nF; 250 V	C10	10 nF; 250 V
C11	2.2 nF; 1 kV	C11	3.3 nF; 1 kV
C12	2.2 nF; 1 kV	C12	4.7 nF; 1 kV
T1	7608000902	T1	760800031

4.11 15 W step dimmable CFL schematic with UBA20261/2

The full schematic of the application with a 15 W step dimmable CFL is shown in Figure 13.

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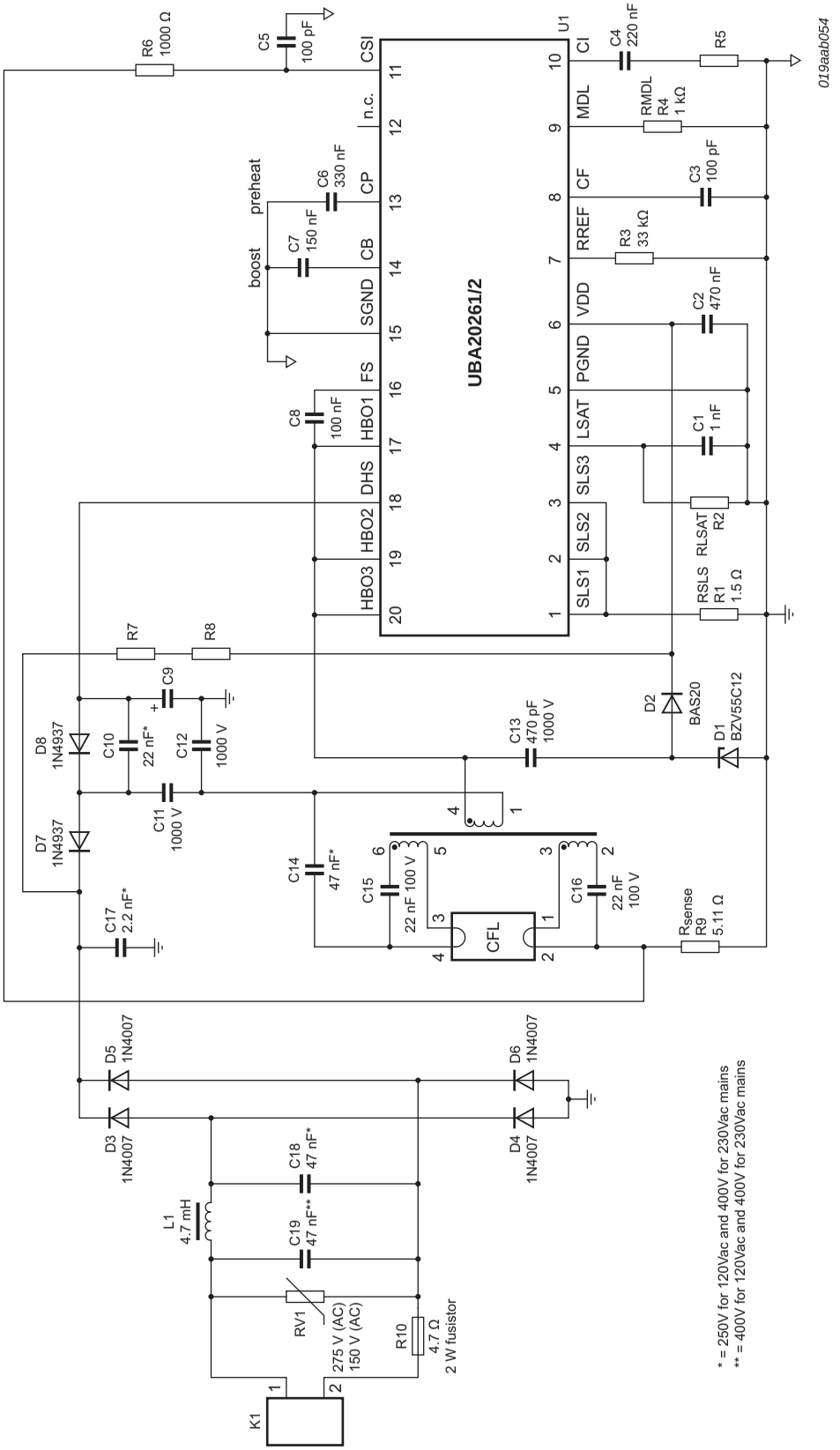

Fig 13. 10 W step dimmable CFL schematic with UBA20261/2

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Table 6. Component values

UBA20261		UBA20262	
Component	**Value**	**Component**	**Value**
R2	100 kΩ	R2	100 kΩ
C9	22 μF; 250 V	C9	6.8 μF; 400 V
C10	10 nF; 250 V	C10	10 nF; 250 V
C11	2.2 nF; 1 kV	C11	3.3 nF; 1 kV
C12	2.2 nF; 1 kV	C12	4.7 nF; 1 kV
T1	760800031	T1	7608000902

4.12 End Of Life circuit (EOL)

The auto-transformer winding can be used for an optional End Of Life (EOL) circuit when:

- T1d is not used as an autotransformer winding
- the winding is placed in series with R_{sense}

The EOL circuit senses a high lamp voltage during operation by sensing the voltage across the lamp inductor L_{res}. An aged (or old lamp) or a lamp which breaks during operation can cause the high voltage

The EOL circuit only works when the IC is in the burn state by pulling the CP pin below 1 V. Adjustment of the circuit can be done by changing the value of R22.

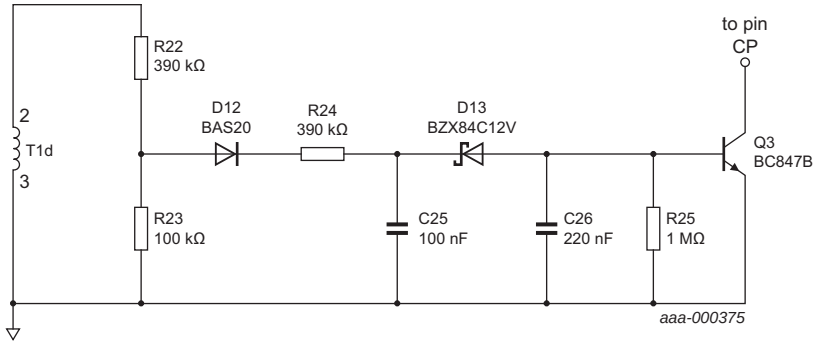

Fig 14. EOL circuit

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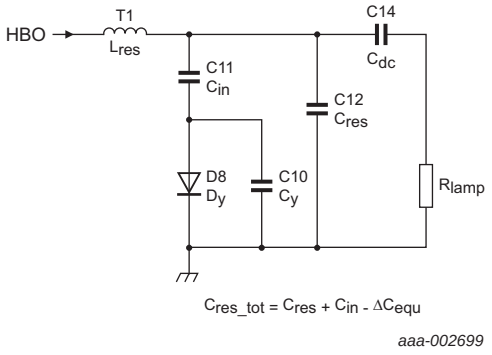
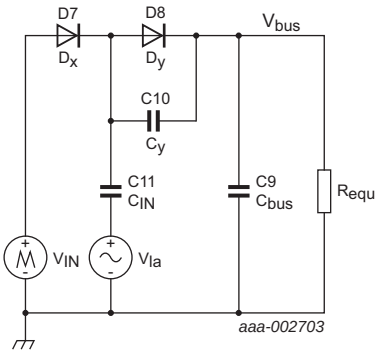
5. Appendix 1: Voltage source charge pump calculations



a. Equivalent resonant tank.



b. Simplified equivalent circuit of Figure 1.

Fig 15. VSCS-CP with enhanced conduction angle design

5.1 Assumptions

- V_{bus} is always higher than the input peak voltage and is ripple free
- The lamp voltage V_{lamp} which is equal to the voltage across C_{res} is considered to be a frequency voltage source
- The rectified line voltage V_{IN} is assumed constant over one switching cycle and the switching frequency f_s is much higher than double the line frequency
- The phase shift between the voltage source V_{lamp} and the current source I_{res} = 90°

5.2 Lamp current crest factor

ΔC_{equ} is maximum difference of equivalent resonant capacitance during different topological stages and is a criterion for determining the crest factor approximately.

$$\Delta C_{equ} = \frac{C_{IN}^{2}}{C_{IN} + C_{res}} \quad (11)$$

$$C_{res(equ)} = C_{res} + \Delta C_{equ} \quad (12)$$

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5.3 Current stress in output stage steady state mode (100 % burn state)

$$I_{ss} \approx \frac{\pi \cdot V_{bus}}{V_{IN(p)}} \cdot L_{IN(p)} \cdot \sqrt{1 + \left(\frac{\eta \cdot V_{IN(p)}{}^2}{2\pi \cdot V_{lamp(p)}}\right)^2 \cdot \left(1 + \frac{C_{res}}{C_{IN}}\right)^2} > \frac{\pi \cdot V_{bus}}{V_{IN(p)}} \cdot I_{I(p)} \quad (13)$$

Where:

- Unity power factor is assumed
- $I_{in(p)}$ = peak line input current
- $V_{IN(p)}$ = amplitude of the line voltage
- $V_{lamp(p)}$ = lamp voltage amplitude in burn state
- η = circuit conversion efficiency in burn state

5.4 DC bus voltage stress during burn state

$$V_{bus(burn)} = \sqrt{\left(\frac{C_{IN}}{C_{IN} + C_y}\right)^2 \cdot 2 \cdot V_{lamp}} \quad (14)$$

5.5 DC bus voltage stress during ignition state

$$V_{bus(max)} = \frac{V_{lamp(p)ign}}{V_{lamp(p)}} V_{bus(burn)} + \frac{\pi}{4} V_{IN(p)} \left[1 - \frac{\frac{P_{loss}}{\left(\frac{P_{rated}}{\eta}\right)}}{\frac{f_{ign}}{f_{burn}}}\right] \quad (15)$$

Where:

- $V_{lamp(p)ign}$ = peak lamp voltage at lamp ignition
- P_{loss} = total loss in ignition phase state
- P_{rated} is the lamps nominal or rated power
- f_{start} = starting frequency
- f_{burn} is the frequency in burn state

Using η = 80 % in the burn state is a good practical value.

5.6 Average input line current and power over one switching cycle

$$I_{IN(avg)} = (C_{IN} + C_Y) \cdot \left[V_{IN} + \frac{C_{IN}}{C_{IN} + C_y} \cdot 2 \cdot V_{lamp(p)} - V_{bus}\right] \quad (16)$$

$$P_{IN(avg)} = \frac{1}{2} \cdot f_s (C_{IN} + C_y) \cdot V_{IN}{}^2 + \frac{2V_{IN(p)}}{\pi} \cdot f_s \cdot (C_{IN} + C_y) \cdot \left[\frac{C_{IN}}{C_{IN} + C_y} \cdot 2 \cdot V_{lamp(p)} - V_{bus}\right] \quad (17)$$

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5.7 Unity PF condition

$$\frac{C_{IN}}{C_{IN} + C_y} \cdot 2 \cdot V_{lamp(p)} = V_{bus} \quad (18)$$

5.8 Input and output power balance

$$C_{IN} + C_y = \frac{2 \cdot P_o}{\eta \cdot f_s \cdot V_{IN(p)}} \quad (19)$$

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6. Appendix 2: Inductive mode preheat calculations

The following values and equations are used for inductive mode preheat calculations. Half-bridge preheat winding are shown in Figure 16.

Where: V_{bus} = 350, $t_{hb} = 10 \cdot 10^{-6}$ and $t_r = 0.5 \cdot 10^{-6}$

t_r is the time it takes to rise from the minimum to maximum value.

$$f_{hb} = \frac{1}{t_{hb}} \tag{20}$$

Where: $f_{hb} = 100 \cdot 10^3$, $\omega_{hb} = 2 \cdot \pi \cdot f_{hb}$ and $\omega_{hb} = 628.319 \times 10^3$

$$\gamma = \frac{t_r}{t_{hb}} \cdot \pi \tag{21}$$

Where: γ = 0.157, m = 1, 2 to 80 and t = 0, $0.001 \cdot t_{hb}$ to $2 \cdot t_{hb}$

$$V_{hb\_f(m)} = j\frac{V_{bus}}{2 \cdot \pi \cdot \gamma} \cdot \frac{(-1)^m - 1}{m^2} \cdot sin(m\gamma) \tag{22}$$

$$V_{hb\_t}(t) = 2 \cdot Re\left[\sum_m (V_{hb\_f}(m) \cdot e^{j \cdot 2 \cdot \pi \cdot f_{hb \cdot m \cdot t}})\right] \tag{23}$$

Figure 16[a] shows that the half-bridge voltage is supplied to the LC filter from which the inductor has two preheat windings. The circuit with the two preheat windings can be redrawn as shown in Figure 16[b].

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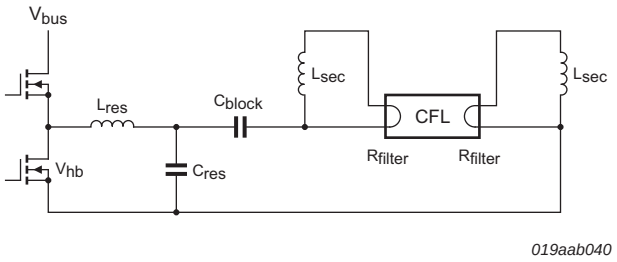
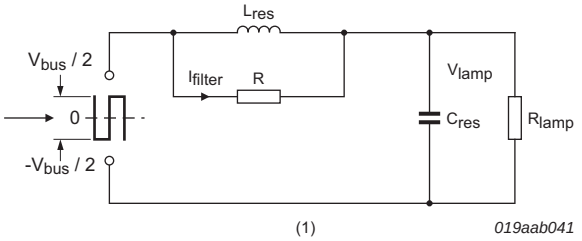


a. Inductor with two preheat windings



(1) Related equations see Equation 24, Equation 25 and Equation 25

b. Reduced circuit with two preheat windings

Fig 16. Half-bridge and preheat windings

$$R = \frac{1}{2}\frac{L_{res}}{L_{sec}}R_{filter} \tag{24}$$

$$R_{lamp} = \frac{V_{lamp}^{2}}{P_{lamp}} \tag{25}$$

Where: $L_{res} = 2.75 \cdot 10^{-3}$, $L_{sec} = 10 \cdot 10^{-6}$, $C_{res} = 4.7 \cdot 10^{-9}$ and $R_{filter} = 50$

$$I_{fil\_f}(m) = \frac{-(m \cdot \omega_{hb})^2 \cdot L_{res} \cdot C_{res} \cdot \sqrt{\frac{L_{sec}}{L_{res}}}}{j \cdot 2 \cdot m \cdot \omega_{hb} \cdot L_{sec} + R_{filter} - (m \cdot \omega_{hb})^2 \cdot L_{res} \cdot C_{res} \cdot R_{filter}} \cdot v_{hb\_f}(m) \tag{26}$$

$$i_{fil(RMS)f} = \sqrt{2 \cdot \left[\sum_m (|i_{fil\_f}(m)|)^2\right]} \tag{27}$$

$i_{fil(RMS)f} = 0.18$

$$i_{fil\_t} = 2 \cdot Re\left[\sum_m (i_{fil\_f}(m) \cdot e^{j \cdot 2 \cdot \pi \cdot f_{hb} \cdot m \cdot t})\right] \tag{28}$$

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7. Abbreviations

Table 7. Abbreviations

Acronym	Description
CFL	Compact Fluorescent Lamp
CSP	Coil Saturation Protection
CMD	Capacitive Mode Detection
EMI	ElectroMagnetic Interference
OCP	OverCurrent Protection
OVP	OverVoltage Protection
PF	Power Factor
PFC	Power Factor Correction
RLC	Resistance, Inductance, Capacitance
SoS	Sum of Squares
UVLO	UnderVoltage LockOut
VCD	Voltage Controlled Oscillator
VSCP	Voltage Source Charge Pump
ZVS	Zero Voltage Switching

8. References

[1] **AN10803 and AN10872 —** Application notes: Triac dimmable CFLs using UBA20260, UBA20261/2, UBA2028 and UBA2014.

[2] **UBA20260, UBA20261/2 —** Data sheet.

[3] **Power factor correction 1989 IEEE —** Current waveform distortion in power factor correction circuits employing discontinuous mode boost converters.

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